Lab Description:

In this lab I constructed a state machine that represent each signal period including init, send, holdoff, listen, wait and measure states. The init is the reset point and the start of the state machine. The send is when the FPGA send a signal to the ping machine. The holdoff is the holding time for FPGA keeps sending the signal. Listen is the 750ms for the ping machine to listen. Wait machine is for the ping machine wait for the pulse. And the measure is the state for the ping machine to listening the send back signal from the object and measure distance. Also, I add three counters for the holdoff, listen and wait.

For the data path logic, the 4 counters measure the duration in the process of holdoff, listen, measure and wait. The comparators for the send, holdoff and wait counters ensure when the counter reaches the exacted value I calculated in the prelab the signal could transfer to the next step. After get the counter value of the measure state, I will multiply with the inch or centimeters I calculate in the prelab and then divided by 2^16 for the value of 23:16 written in the lab manual, which is the final result of this lab.